ST. ANNE'S

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QUESTION BANK

PERIOD: JUNE 2019 – DEC 2019 **BATCH**: 2017 – 2021

BRANCH : CSE **YEAR/SEM:** III/V

SUBJECT: EC 8691 Microprocessors and Microcontrollers

UNIT-I (The 8086 Microprocessor)

1. **What is Microprocessor?**

   Microprocessor is a program controlled semiconductor device (IC), which fetches, decode and executes instructions.

2. **What are the basic units of a microprocessor?**

   The basic units or blocks of a microprocessor are ALU, an array of registers and control unit.

3. **What is assembly language?**

   The language in which the mnemonics (short -hand form of instructions) are used to write a program is called assembly language. The manufacturers of microprocessor give the mnemonics.

4. **Define bit, byte and word.**

   A digit of the binary number or code is called bit. Also, the bit is the fundamental storage unit of computer memory. The 8-bit (8-digit) binary number or code is called byte and 16-bit binary number or code is called word. (Some microprocessor manufactures refer the basic data size operated by the processor as word).

5. **What is a system bus? (May 2015)(Dec 2016)(Nov/Dec 2018)**

   Bus is a group of conducting lines that carries data, address and control signals.

6. **Why data bus is bi-directional?**

   The microprocessor has to fetch (read) the data from memory or input device for processing and after processing, it has to store (write) the data to memory or output device. Hence the data bus is bi-directional.

7. **Why address bus is unidirectional?**

   The address is an identification number used by the microprocessor to identify or access a memory location or I / O device. It is an output signal from the processor. Hence the address bus is unidirectional.

8. What is the machine cycle of microprocessor in a system? (Dec 2016)

A machine cycle also called a processor cycle or a instruction cycle is the basic operation performed by a microprocessor.

9. Name the software operation possible with the 8086 compared with 8085 microprocessor (Nov/Dec 2005)

1. Byte and word multiply and divide , Block moves and compares
2. Software interrupts, Multiprocessor coordination
3. Byte transactions, Nondestructive bit testing
4. Program loop instructions

10. What are the difference between 8085 and 8086 processor? (Nov/Dec 2013)

8085 Microprocessor	8086 Microprocessor
It is 8-bit Microprocessor	It is 16-bit Microprocessor
It has 16-bit address line	It has 20-bit address line
It has 8-bit data bus	It has 16-bit data bus
It has 5 flags	It has 9 flags
It does not support pipe-lining	It support pipe-lining
It does not support memory segmentation	It support memory segmentation

11. Write the special functions carried out by the general purpose registers of 8086.

- AX- 16 bit accumulator, AL- 8 bit accumulator
- BX- Base register , CX- Count register
- DX- Data register

12. List out the segment registers of 8086. (Nov/Dec 2008, Nov/Dec 2004, Dec 2016)

i. Code segment register

ii. Data segment register

iii. Stack segment register

iv. Extra segment register

13. State the functional units available in 8086. (Nov/Dec 2004)

BIU (Bus Interface Unit)

EU (Execution Unit)

14. What is the flag register in 8086? (May 2009, Dec 2016)(May 2019)

A flag is flip-flop which indicates some condition produced by the execution of an instruction or controls certain operation of the Execution Unit.

Flag register is a 16-bit register containing nine 1-bit flags:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

				OF	DF	IF	TF	SF	ZF		AF		PF		CF

Six status or condition flags (OF, SF, ZF, AF, PF, CF)

Three control flags (TF, DF, IF)

15. What is the function of T and D flags in 8086? (April/May 2005)

D Flag-String Direction Flag:

It is used to set direction in string operation.

T Flag - Single Step Trap Flag:

It is used for single stepping through a program.

16. What is the role of TF and IF flags in the flag register of 8086? (Nov/Dec 2004)

(i) TF (Trap Flag)

Setting TF puts the 8086 in the single step mode. In this mode, the 8086 generates an internal interrupt after execution of each instruction.

(ii) IF (Interrupt Flag)

Setting IF causes the 8086 to receive external maskable interrupts through INTR pin. Clearing IF disables these interrupts.

17. What is the function of bus interface unit? (Nov/Dec 2008)

The bus interface unit (BIU) interfaces the 8086 with external devices including memory via the bus. BIU fetches instructions, reads data from memory and ports, and writes data to memory and I/O ports.

18. What are maximum address space and data bus width of 8086 processor? (Nov/Dec 2008)

Maximum address space $= 2^{20} = 1$ MB

Data bus width - 16 bit

19. What information is conveyed when $QS_1 - QS_0$, bits are 01? (April/May 2008)

The queue status lines ($QS_1 - QS_0$) give information about the status of the code.

QS, - $QS_0 = 01$ indicates the first byte of opcode from queue.

20. What happen in 8086 when $\overline{DEN} = 0$ and DT/$\bar{R} = 1$? (April/May 2008)

$\overline{DEN}$ and DT/$\bar{R}$ signals are used for buffering the data. The data enable $\overline{DEN}$ signal informs the transceivers (8286 / 8287) that the 8086 is ready to transmit or receive data. When $\overline{DEN}$ = 0 and DT/$\bar{R}$ = 1, 8086 is ready to transmit the data to transceivers.

21. What is the storage space required to store the interrupt vectors of 8086. (April/May 2008)

In 8086, 256 interrupt types required (256 x 4) 1024 bytes storage space.

22. What is pipelining in an 8086 processor? (Nov/Dec 2004)

Feature fetching the next instruction while the current instruction executes is called pipelining. The 8086 BIU fetches six instruction bytes ahead of time from the memory and save pre-fetched instructions in queue to implement pipelining.

23. What is a queue? How queue is implemented in 8086? (April/May 2004)

A data structure carried by the registers on the basis of first-in-first-out (FIFO) is called queue.

The 8086 have six numbers of 8 bit FIFO registers, which is used for instruction queue.

24. What is the function of Instruction pointer (IP)?

IP is also referred as program counter. It is used in the calculation of actual memory address of instruction. It stores the offset for the instruction.

25. What is the operation carried out when 8086 executes the instruction MOVSW? (April/May 2005)

MOVSW - Move word string.

This instruction transfers a word from the source string (addressed by SI) to the destination string (addressed by DI) and updates SI and DI to point to the next string element.

26. What is the string ans byte instruction executed by 8086?(Nov/Dec 2018)

MOVSB - Move String Byte

Move 8 bit data from memory location addressed by SI in segment DS location addressed by DI in segment ES. [DI]← [SI]

If DF (Direction Flag) = 0, SI is incremented by 1

= 1, SI is decremented by I

27. What do these 8086 instructions do? STD, IRET. (Nov / Dec 2007)

STD - Set the direction flag in flag register (D=l)

IRET- Interrupt on Return. It is used to exist any interrupt procedure, whether activated by software or hardware.

28. List any four unconditional branch instructions. (Nov/Dec 2007)

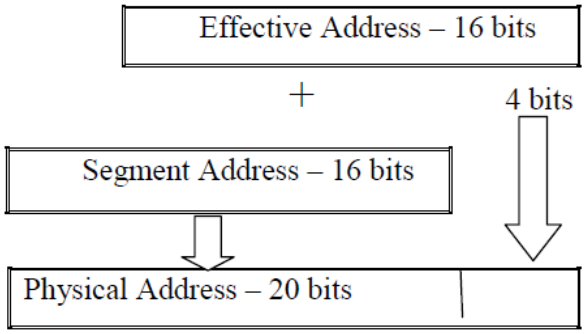
CALL, JMP, RET, LOOP

29. Name any four processor control instructions (8086). (April/May2005)

1. CLC
2. CMC
3. STC
4. STD
5. WAIT
6. HLT
7. LOCK
8. NOP

30. How the 20 bit effective address is calculated in an 8086 processor? (April/ May 2006)

Effective address = (segment address x 10H) + offset address.



31. How the physical address for fetching the next instruction to be executed is obtained in 8086? (Nov/Dec 2005)

The physical address is obtained by appending four zeros to the content present in CS register and then adding the content of IP register with the above value.

CS => 16 bit content + 0000

IP => 0000+ 16 bit content

Physical address => 20 bit address

For example, assuming the content of

CS = 1200H

IP = 0345 H '

CS = 0001 0010 0000 0000 0000

IP = 0000 0011 0100 0101

0001 0010 0011 0100 0101

Physical address : 12345 H

32. Define segment override prefix. (May/June 2009, May/June 2007, Nov/Dec 2004)

- Segment override prefix can be used in any instruction with any memory addressing mode to override the default segment register. Most memory instructions use DS as the default segment register.
- A segment override prefix allows any segment register (DS, ES, SS or CS) to be used as the segment when evaluating addresses in an instruction.

33. If the execution unit generates an effective address of 43A2 H and the DS register contains 40000 H. What will be the physical address generated by the BIU? What is the maximum size of the data segment? (May/June 2009, Nov/Dec 2015)

Effective address = 43A2 H

Physical address = 40000 H

443A2 H

Maximum size of DS - 2^{16} = 64 K bytes

34. Mention the addressing modes of the 8086: (Nov/Dec 2008,MAY 2015,2018)

Immediate, Direct, Register, Register Indirect, Indexed, Register Relative addressing modes

35. What is the addressing mode of the following instructions?(April/May 2008, MAY 2015)

(i) **JMP [3001 H] -** Inter segment indirect addressing mode

(ii) **MOV AX, 55H [BX] [SI] -** Relative based indexed addressing mode.

36. The CS contains A820, while the IP contains CE24. What is the resulting physical address?

(Nov/Dec 2008)

Segment address	A	8	2	0	
Offset address		C	E	2	4
Physical address	B	5	0	2	4

The physical address is B5024 H.

37. What is an assembler directive? Give an example. (April/May 2011)(May/June 2012)

An assembler directive is a statement to give direction to the assembler to perform the task of assembly process. Example: EQU, DUP, LENGTH, OFFSET, LABEL

38. Give the importance of assembler directive EVEN. (Nov/Dec 2011)

Using EVEN directive, the next data item or label is made to start at the even address boundary. The assembler, on encountering EVEN directive, will advance the location counter to even address boundary. For example:

- EVEN TABLE DW 20 DUP (0)

This statement declares an array named TABLE of 20 words starting from the even address. Each word is initialized to zero.

39. Write a program that will carry out the following binary operation using instruction.

W=X + Y + 24-Z (Nov/Dec2004)

```
MOV   AX,X
ADD   AX, Y
ADD   AX, 24
SUB   AX, Z
MOV   W, AX
```

40. What is Macro? (Nov/Dec 2007) (May 2019)

Macro is a short sequence of instructions. It is a small subroutine. A macro can be defined anywhere in a program using the directives MACRO and ENDM.

41. What do you mean by non maskable interrupt? (Nov/Dec 2008)

Non-Maskable interrupt (NMI) is the highest priority hardware interrupt that triggers on, the positive edge. This interrupt cannot be disabled or masked. It is used to save program data or processor status in case of system power failure.

42. What is meant by software interrupt in 8086? (May/June 2007, April/May 2005)

The software interrupts are program instructions. These instructions are inserted at desired locations in a program. While running a program, if a software interrupt is encountered then the processor executes an interrupt service routine (ISR).

43. Why is an interrupt driven I/O more efficient than programmed I/O for 8086 microprocessor? (Nov/Dec 2005)

i. Interrupt I/O uses the built in interrupt capabilities.

ii. Interrupt I/O is asynchronous in nature.

iii. Programmed I/O is special I/O program which is in full control of data transfers. Using a software technique called polling, the microprocessor is synchronized to the speed of the peripheral. It is inefficient due to continuous status check.

iv. Processor responds to the peripheral only when ready and efficient became there is no need to poll the status.

44. The offset address of a data is $341B_H$ and the data segment register value is $123A_H$. What is the physical address of the data?(May 2017)

Offset address = 341B H

Segment address = 123A H

Physical Address = 157BB H

45. An interrupt device based on 8086 microprocessor sends 03 H onto AD_O thru AD_7 data bus when $\overline{INTA}$ is low. Where should the interrupt jump address located in the vector table? (Nov/Dec 2005)

When INTA is low, data gated to microprocessor = 03 H

The interrupt jump address has to be loaded at location = 03 x 4bytes.

= 12 = OCH

Therefore, the starting address of interrupt = 000CH

The ending address of interrupt = 000F H

46. What are the different between macros and procedures? (April/May 2006)

S.No	Procedures	Macros
1	To use a procedure use ALL and RET instruct are needed	To use macro, just type its name
2	It occupies less memory.	It occupies more memory.
3	Stack is used.	Stack is not used.
4	To mark the end of the procedure, type the n of the procedure before the ENDP directive.	To mark the end of the macro ENDM directive is enough.
5	Overhead time is required to call the proce and return to the calling program.	No overhead time during the execution

47. What is called an interrupt in 8086?(Nov/Dec 2018)

A signal to the processor to halt its current operation and immediately transfer the control to interrupt service routine (ISR) is called an interrupt. Interrupt are triggered either by hardware or software.

48. What is the use of interrupt vector table in 8086?

Interrupt vector table is a table maintained by the operating system. It contains the addresses of the current interrupt service routine. When an interrupt occurs the processor branches to the address in the table that corresponds to the interrupt number.

49. Name the hardware interrupts of 8086. (May/June 2013)

INTR – Interrupt Request

NMI – Non Maskable Interrupt

50. What is the BIOS function call in 8086? (April/May 2011)

Basic Input Output System (BIOS) is used as a software interface between assembly language programs and computer system hardware.

The BIOS services consists of a set of device memory and process control services that are available to any program which is capable of setting register and invoking software interrupts.

51. Define Stack pointer. (May 2018)

Stack segment is a 16-bit register containing address of 64KB segment with program stack.

By default, the processor assumes that all data referenced by the stack pointer (SP) and base pointer (BP) registers are located in the stack segment.

52. What is the use of assembler?

An assembler program is used to translate the assembly language mnemonics for instructions to the corresponding binary codes.

PART-B

1. Explain the features of 8086 microprocessor. (May 2011, 8 Marks)(or)How microprocessor is different from microcomputers. .(Nov/Dec 2018) **(May 2019)**
2. Explain the internal architecture of 8086 microprocessor.(May 2015) **(Dec 2017,May 2017,2018,2019)**
3. What are the addressing modes in 8086? Explain with example.(Nov/Dec 2016,2017,2018)
4. Explain the instruction set of 8086 microprocessor.

   Give three examples for the following 8086 microprocessor instructions: String Instructions,

   Process Control Instruction, Program Execution Transfer Instructions and Bit manipulation

   Instructions. (May 2010)(June 2016)

   Explain the data transfer, arithmetic and branch instructions with examples. (June 2016) .(Nov/Dec 2018)
5. Explain the assembler directives in 8086 Microprocessor. (Dec-2006, 11, 12, May2007, 08,10,11,13, Dec 2016).
6. Write a program based on 8086 instruction set to compute the average of 'n' number of bytes stored in the memory.(Nov/ Dec 2012)
7. Write an 8086 ALP to sort the array of elements in ascending order. (Apr/ May 2011, May / June 2013)
8. Write an 8086 ALP to find the largest element in array elements. (Apr/ May 2011)
9. Write an 8086 program to convert BCD data to binary data. (Nov/ Dec 2010) **(**May 2015)

10. Explain linking and relocation concepts in 8086 Processor.
11. Define macro. Explain how macros are constructed in ASM-86 with example.(Dec-2010, May2006,10,11)
12. What are the interrupts in 8086? Explain interrupt related service routines.(Dec-2007,08,12, May-2007,08,11,12,13,15, May 2016, May 2017,2018,2019)
13. Write a program to perform basic arithmetic operations using 8086.
14. Write a program to perform basic logical operations using 8086.
15. How stacks are accessed in 8086 processor? Explain briefly. (Dec-2007)

UNIT-II 8086 SYSTEM BUS STRUCTURE

1. What does it imply if the states of 8086 signals - $\overline{BHE}$ and A_0 are at 0 and 1, respectively. (Nov/Dec 2008)

When $\overline{BHE}$ = 0 and A_0=l, 8086 can access even byte address (D_o - D_7)

2. What is the function of LOCK and RQ/GT signal? (May/June 2013)

LOCK- This signal indicates that an instruction with lock prefix is being executed and the bus is not to be used by any other processor.

RQ/GT- In maximum mode DMA request is received and acknowledged using these signals.

3. Explain the BHE and LOCK signal of 8086. (April/May 2008)

- BHE - Bus High Enable signal is used to indicate the transfer of data over the higher order (D_8-D_{15}) data bus.
- LOCK - Lock signal locks the bus from being relinquished for DMA or other bus masters.

4. What is the use of HOLD and HLDA signals? (Nov/Dec 2007)

HOLD - This signal indicates that another master is requesting the host 8086 to handover the system bus.

HLDA - (Hold acknowledge) - On receiving HOLD signal, 8086 outputs HLDA signal high as an acknowledgement.

5. State the modes in which 8086 operate. (May/June 2007, Nov/Dec 2004,2017)

- ✓ Minimum mode
- ✓ Maximum mode

6. What is the purpose of CLK signal in an 8086 system? (Nov/Dec 2006)

The clock signal provides the basic timing for processor operation and bus control activity. The clock frequency may be 5 MHz or 8 MHz of 10 MHz for different 8086 versions.

7. Name the signals used by 8086 to demultiplex the address/ data bus. (Nov/Dec 2005)

The signals used by 8086 to demultiplex the address/data bus are $\overline{BHE}$, A_0 and ALE

$\overline{BHE}$	A_0	
0	0	Access 16 bit word
0	1	Access odd byte D_8-D_{15}
1	0	Access even byte D_0-D_7
1	1	No action

8. Name the signals used by 8086 to control the data bus buffers. (Nov/Dec 2005)

In minimum mode of operation,

DT/$\bar{R}$ - Data transmit/receive

DEN -Data enable

In maximum mode of operation

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	**Function**
0	0	0	$\overline{INTA}$
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Code access
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

9. State the function of queue status lines QS0 **and** QS1 **in 8086 microprocessor?**

QS0 and QS1 signals are decoded to provide instruction queue status.

QS1	**QS0**	**Decoded function**
0	0	Queue is in idle state
0	1	First byte of opcode has entered queue
1	0	Queue empty
1	1	Subsequent byte of opcode has entered queue

10. Give the function of the following 8086 CPU pins. (Nov/Dec 2005)

a) MN/$\overline{MX}$ b) LOCK (DEC 2017)

MN/$\overline{MX}$:

This pin configures CPU in minimum mode when strapped HIGH and in maximum mode when strapped LOW.

LOCK :

It locks the bus from being relinquished for DMA or other bus masters.

11. What is the function of $\overline{TEST}$ Pin in 8086 processor? (April/May 2005)

TEST Pin is used to check the status of software (through the TEST instruction). If the TEST output is LOW, execution continues otherwise it waits until it goes to LOW.

12. What is the function of the following signal pins in 8086 based systems:

$\overline{BHE}$ MN/$\overline{MX}$, TEST and RESET (April/May2004)

$\overline{BHE}$ -Bus High Enable. Low signal on this pin indicates that atleast one byte of the current transfer is to be made on higher order byte AD_8-AD_{15}; otherwise the transfer is made on lower order byte AD7-AD0.

MN/$\overline{MX}$ - If MN/MX = 1, 8086 can be configured in minimum mode. If MN/$\overline{MX}$ = 0, 8086 can be configured in maximum mode.

TEST - TEST Pin 's used to check the status of software (through the TEST instruction). If the TEST outputs LOW, execution continues otherwise it waits until it goes to LOW.

RESET - It clears PSW, IP, DS, SS, ES and the instruction queue.

13. Distinguish between maximum mode and minimum mode of operation of 8086 processor?(May 2018)

S.No	Maximum Mode	Minimum Mode
1	For maximum mode operation $MN/\overline{MX}$ pin is grounded	For Minimum mode operation $MN/\overline{MX}$ pin is connected to V_{cc}
2	An external bus controller (Intel 8288) is used to generate bus control signal.	All control signals are generated inside 8086 microprocessor.
3	Works in multiprocessor mode.	Works in uniprocessor mode

14. Give the operation of CBW and TEST instructions of 8086. (Nov/Dec 2013)

CBW

This **(Convert Byte to Word)** instruction converts a byte to a word. It extends the sign of the byte in register AL through register AH.

TEST

TEST destination, source

This (TEST) instruction performs the logical "AND" of the two operands and updates the flags but does not store the result.

(DEST) "AND" (SRC)

15. Define interfacing. (Dec 2004)

Interfacing is the method used to interconnect two separate electronic devices in such a way that their output and input voltage and currents are compatible.

16. What is the need for interfacing? (May 2006)

To communicate with external world, microprocessor needs interfacing with peripheral storage devices, input and output devices and display devices.

17. What is programmed I/O?

Programmed I/O consists of continually examining the status of an interface and performing an I/O operation with the interface when its status indicates that it has data to be input or its data-out buffer register is ready to receive data from the CPU.

18. In what ways are the standard microprocessor and co-processor differ from each other? (Nov/Dec 2012)

Co-processor performs their job under the control of microprocessor.

19. How does coprocessor identify the instruction meant for it? (April/May 2011,ND 2017 2018)

The initial codes are decoded by the processor and it has four ones (MSB) then it is mean for coprocessor otherwise processor will execute.

20. Explain why the processor utilization rate can be improved in a multiprocessor system by an instruction queue. (May 2008)

The processor has to fetch the instruction from memory before decode and execute it. Fetching the instruction from memory takes considerable amount of time and processor has to wait during this time, reducing its utilization rate. The instruction queue mechanism fetches the few nest instructions before the execution of current instruction so that the processor need not have to wait for instruction fetch, improving the utilization rate.

21. What are loosely coupled systems? (May 2019)

In loosely coupled systems each CPU may have its own bus control logic. The bus arbitration is handled by an external circuit, common to all processors. The loosely coupled system configuration like LAN & WAN can be spread over a large area.

22. What are the three basic multiprocessor configurations that the 8086 can support? (May/June 2009, Nov/Dec 2003)

1. Coprocessor Configuration
2. Closely Coupled Configuration
3. Loosely Coupled Configuration

22. What are the advantages of a loosely coupled configuration in a multiprocessor system? (April/May 2006, April/May 2004) (May 2019)

4. Each processor may have a local bus to access local memory or I/O devices so that a greater degree of parallel processing can be achieved.
5. More flexible.
6. Better system throughput by having more than one processor.
7. If any fault occurs in a module, that faulty module can be detected and replaced. So the breakdown of the entire system is avoidable.

23. Compare closely coupled configuration features with loosely coupled configuration features. (May/June 2012) (May/June 2012)

Closely coupled system:

1. Share memory multiprocessor system.
2. Several processors share a common memory.
3. Processor communicates through shared memory.

Loosely coupled system:

Distributed memory multiprocessor.

8. Each processor has its own local memory.

Processors are tied tighter by switching through message passing scheme.

24. What are the features of closely coupled multiprocessor system? (Nov/Dec 2010)

1. The MP may share a common clock and bus control logic.
2. The two processors in a closely coupled system bus or common memory.

25. Name the three bus allocation schemes used in loosely coupled multiprocessor system. (Nov/Dec 2003)

1. Daisy Chaining
2. Polling method
3. Independent Request

26. What is meant by Daisy chaining method?

It does not require any priority resolving network, rather the priorities of all the devices are essentially assumed to be in sequence.

All the masters use a single bus request line for requesting the bus access. The controller sends a bus grant signal, in response to the request, if the busy signal is inactive when the bus is free. The bus grant pulse goes to each of the masters in the sequence till it reaches a requesting master .The master then receives the grant signal, activates the busy line and gains the control of the bus. The priority is decided by the position of the requesting master in the sequence.

27. What is independent bus request scheme?

Each of the masters requires a pair of request and grant pins which are connected to the controlling logic. The busy line is common for all the masters. . f the controlling logic receives a request on a bus request line, it immediately grants the bus access using the corresponding bus grant signal, provided the BUSY line is inactive, and then grants the request. This is quite fast, because each of the masters can independently communicate with the controller.

28. What is meant by polling?

In polling schemes, a set of address lines is driven by the controller to address each of the masters in sequence. When a bus request is received from a device by the controller, it generates the address on the address lines. If the generated address matches with that of the requesting masters, the controller activates the BUSY line.

29. Name some of the advanced 8086 microprocessors and its features. (May 2017,Dec 2017)

The Intel 80386 - were included a 32-bit data bus structure and the ability to address up to 4GB of memory.

The Intel 80486 - was a 32-bit data bus structure, and the ability to address up to 64GB of memory.

The Pentium II processor - was a 7.5 million-transistor, it incorporates the Pentium pro and the Intel MMX technology, which is designed specifically to process video, audio and graphics data efficiently.

30. What is meant by multiprogramming?(May 2017,May 2018)

Multiprocessor Systems refer to the use of multiple processors that execute instructions simultaneously and communicate using mailboxes and semaphores Maximum mode of 8086 is designed to implement 3 basic multiprocessor configurations:

1. Coprocessor (8087)
2. Closely coupled (dedicated I/O processor: 8089)
3. Loosely coupled (Multi bus)

31. What are the types of I/O programming?

The principal types of I/O programming are

1. Programmed I/O
2. Interrupt I/O 3. Block transfers

PART-B

1. Explain the signal used in 8086 processor. (Dec 2003,06,07,09,10,13, May 2006,07,08,09,11)
2. Explain with neat diagram minimum mode configuration of 8086 system. (Dec 2006, 08, May 2006,2019)
3. Explain with neat diagram maximum mode configuration of 8086 system. (Dec 2007) **(May 2019)**
4. Draw and explain the timing diagram of different cycle in 8086 processor. (Dec 2007, May 2009, 13, Dec 2016, May 2017)
5. With example explain the input output program concepts in 8086.
6. Explain the different configurations of multiprocessor systems. (May 2008)
7. Explain multiprocessor system. (June 2016, Dec 2016,2017)
8. Explain how co processor works and interacts with 8086. (June 2016)
9. Explain the closely coupled configuration of 8086 with example. .(Nov/Dec 2018)
10. Write brief note on 8086 loosely coupled system configuration. (April 2006, May 2017,DEC 2016)

11. Explain the basic bus access control and arbitration schemes used in multiprocessor systems. **May 2018** (Dec 2016, 2017)
12. Explain the Interrupts Of 8086**(2019)**
13. Explain the Signal Description of 80286.

UNIT 3

I/O INTERFACING

1. What are the requirements to be met while interfacing I/O devices to microprocessor microcontroller? (April/May 2005)/(AU May 2013)

1. The microprocessor identifies the I/O devices through a port address and enables the Read or Write operations.
2. The microprocessor selects the I/O devices through a chip select and uses the control signals Read to receive data and Write signal to transmit data.

2. Compare peripheral I/O and memory mapped I/O.

Peripheral I/O	Memory mapped I/O
I/O devices are treated s input/output and memory is treated as memory.	Booth the devices are treated as input / output and memory.
The control signal used for I/O are IOR and IOW.	The control signals used for I/O are MEMR and MEMW.
Whole address space is available	Less memory space is available due to portioning.
It requires special instruction like IN and OUT.	Instructions available are LDA, STA, LDAZ, STAX, MOV M, ADD A etc. No special instructions are required.
The length of IN and OUT instructions is less so lesser is the execution time.	As the length of instruction like STA, LDA is higher so high is the exaction time.
8bit device address is used.	16bit address is used in this scheme.
Data is transfer only between accumulator and I/O port	Data transfer between any general-purpose register and I/O port
The I/O map is independent of the memory map 256 input device and 256 output device can be connected.	The memory map (64K) is shared between I/O device and system memory

3. What are the advantages and disadvantages of memory mapped I/O?

Advantage: Using 16 bit address for both memory and I/O port.

Disadvantages: Using more instructions instead of IN and OUT instructions.

4. How many address lines in 4096 x 8 EPROM CHIP?

12 address lines

5. Name any four electronic devices which are used to interface high power devices with microprocessor.(Nov/Dec 2004)

1. Power transistor
2. Power MOSFET
3. Solid state relay

6. Define interfacing. (Nov/Dec 2004)

Interfacing is the designing of logic circuits (i.e. Hardware) and writing the instructions (i.e. Software) to enable the microprocessor to communicate with I/O devices.

An interface is a shared boundary between the devices which involves sharing information. Interfacing is the process of making two different systems communicates with each other.

The primary function of memory interfacing is that the microprocessor should be also to read from and write into a given register of a memory chip. To perform these operations microprocessor should

- Be able to select the chip
- Identify the register
- Enable the appropriate buffer.

7. What is memory mapping?[NOV/DEC 2007]

The assignment of memory addresses to various registers in a memory chip is called as memory mapping.

8. What is I/O mapping? [NOV/DEC 2007]

The assignment of address to various I/O devices in the memory chip is called as I/O mapping.

9. Differentiate between absolute and linear select decoding.

Absolute decoding	**Linear decoding**
All higher address lines are defined to select the memory or I/O device	Few higher address lines are decoded to select the memory or I/O device
More b/w is required to design decoding logic	Hardware is required to design decoding logic is less.
Higher cost for decoding circuit	Less cost for decoding circuit
No multiple address	Has a disadvantage of multiple addressing
Used in large systems	Used in small systems.

10. How many address lines and data lines are necessary for accessing 32Kx8 memory? (AU Nov 2011)

15X8=120 Address lines.

11. Define PPI. (Nov/Dec 2004)

PPI is Programmable Peripheral Interface. It is a programmable parallel I/O device. It can be programmed to transfer data between microprocessor and I/O devices under various conditions.

12. What are the basic modes of operation 0f 8255?[APRIL/MAY 2008,Dec 2015] May 2019

There are two basic modes of operation of 8255, viz

a) I/O Mode
   i. Mode 0 – Simple Input/output
   ii. Mode 1 – Strobed Input/output (Handshake mode)

iii. Mode 0 – Strobed bidirectional mode

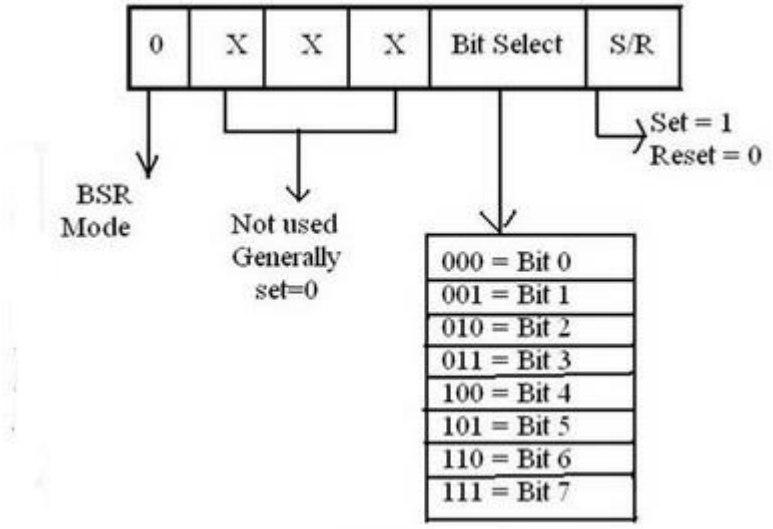
b) Bit Set/Reset Mode

In I/O mode, the 8255 ports work as programmable I/O ports, while In BSR mode only port C (PC0 – PC7) can be used to set reset its individual port bits.

13. Specify the bit which differentiates between I/O mode and the BSR mode in 8255.

If D7 = 1, I/O mode D7= 0, BSR mode

14. Write the word format for BSR mode?



15. Write the features of mode 0 in 8255?

- Two 8- bit ports (port A and port B) and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combined used as a third 8-bit port
- Any port con be used as an input or output port
- Output ports are latched. Input ports are not latched.
- A maximum of four ports are available so that overall 16 I/O configurations are possible.

16. What are the features used mode 1 in 8255?

Two groups – group A an group B are available for strobe data transfer.

- Each group contains cone 8-bit data I/O port and one 4-bit control/data port.
- The 8-bit data port can be either used as input or output port. The inputs and outputs both are latched.
- Out of 8-bit port C, PC0-PC2 is used to generate control signals for port B and PC3 = PC5 are used to generate control signals for port A. The lines PC6, PC7 may be used as independent data lines.

17. What are features used mode 2 in 8255?

The single 8-bit port in-group A is available.

The 8-bit port is bi-directional and additionally a 5-bit control port is available.

Three I/O lines are available at port C, viz PC2-PC0

Inputs and outputs are both latched.

The 5-bit control port C(PC3 = PC7) is used as independent data lines.

18. What is the purpose of control word written to control register in 8255?[APRIL/MAY 2011]

The control words written to control register specify an I/O function for each I/O port. The bit D7 of the control word determines either the I/O function of the BSR function.

19. What is the size of ports in 8255?

Port – A: 8-bits

Port – B: 8-bits

Port – CU: 4-bits

Port – CL: 4-bits

20. What is the purpose of control word written to control register in 8255?

The control words written to control register specify an I/O function for each I/O port. The D7 of the control word determines either the I/O function of the BSR function.

21. What is a control word?

It is a word stored in a register (control register) used to control the operation of a program digital device.

22. Can an input port and an output port have the same port address? [APR / MAY 2010].

No, in peripheral mapped input / output, the peripheral is defined with an 8 bit address input and output devices are different. So, different ports are assigned as input and output port.

23. What is handshake port? (Nov/Dec 2003)

The port used for exchanging the signals between I/O devices and port or between port and processor for checking or informing various condition of the device is called handshake port.

24. What is an USART? (Nov/Dec 2004)

USART - Universal Synchronous/Asynchronous Receiver/Transmitter

The Intel 8251 (USART) is the hardware device that converts parallel to serial data and vice-versa and overcomes such overburden of large program. Hence it is called Programmable Communication Interface.

It is a programmable communication interface that cans communication by using either synchronous or asynchronous serial data.

25. List the uses of USART. (Nov/Dec 2007April/May2005)

- USART provides serial communication
- USART functions are integrated into standard PC interface chip.
- Used in GPS navigation system.
- Mobile applications
- Industrial and control applications

26. What is the use of 8251 chip?

Intel's 8251 A is a universal synchronous asynchronous receiver and transmitter comparable with Intel's Processors.

This may be programmed to operate in any of the serial communication modes built into it. This chip converts the parallel data into a serial stream of bits suitable for serial transmission. It is also able to receive a serial stream of bits and converts it into parallel data bytes to be read by a microprocessor. 8251 chip is mainly used as the asynchronous serial interface between the processor and the external equipment.

27. What is the use of modem control unit in 8251?

The modem control unit handles the modem handshake signal do coordinate the communication between the modem and the USART.

28. What are the functional types used in control words of 8251?

The control words of 8251 A are divided into two functional types.

Mobile Instruction control word

Command Instruction control word

Mode Instruction control word:-

This defines the general operational characteristics of 8251 A.

Command Instruction control word:-

The Command Instruction controls the actual operations of the selected format like enable transmit/receive, error reset and modern control.

29. What are the functions performed by Intel 8251?

8251 is used for converting parallel data to serial data or vice versa. The data transmission or reception can be either asynchronous or Synchronous. It is used to interface MODEM and establish serial communication through MODEM over telephone lines.

30. What are the signals and instructions available in 8085 processor for serial input / output communication? [NOV / DEC 2010]

Signals for serial I/O communication.

SID → Serial Input Data
SOD →Serial Output Data.

Instruction

SIM→Set Interrupt Mask.
RIM→ Read Interrupt Mask.

31. List the features of 8251.(May/June 2007)

It is an universal synchronous and asynchronous communication Controller.
It supports standard asynchronous protocol with a. 5 to 8 bit

Character Format.
Odd, even or no parity generation and detection.
Automatic break detect and handling.

It has built-in Baud rate-Generator
It allows full duplex transmission
It provides error detection logic, which detects parity, overrun and framing errors.
It has 28 pins; DIP package is available.

32. List out three of data transmission.(Nov/Dec 2008)

- Simplex
- Half duplex
- Full duplex

33. What are the different types of methods used for data transmission?

What do you mean by Simplex and Duplex transmission?(April/May 2005)

The data transmission between two points involves unidirectional or bi-directional transmission of meaningful digital data through a medium. There are basically there modes of data transmission.

(a) Simplex
(b) Duplex
(c) Half Duplex

Simplex Transmission:

In simplex mode, data is transmitted only in one direction over a single communication channel.

Example:

A computer (CPU) may transmit data for a CRT display unit in this mode.

Duplex Transmission

In duplex mode, data may be transferred between two transceivers in both directions simultaneously.

Example:

Telephone

Half Duplex Transmission

In half duplex mode, on the other hand, data transmission may take place in either direction, but at a time data may be transmitted only in one direction

Example:

A computer may communicate with a terminal in this mode. When the terminal, sends data (i.e. terminal is se3nder). The message is received by the computer (i.e. the computer is receiver). However, it is not possible to transmit data from the computer to terminal and from terminal to the computer simultaneously.

34. What are the various programmed data transfer methods?

- Synchronous serial data transmission
- Asynchronous serial data transmission
- Interrupt driven data transfer

35. What is synchronous data transfer?

It is a data method which is used when the I/O device and the microprocessor match in speed. To transfer a data to or from the device, the user program issues a suitable instruction addressing the device. The data transfer is completed at the end of the execution of the instruction.

36. What is asynchronous data transfer?

It is a data transfer method which is used when the speed of an I/O device does not match with the speed of the microprocessor. Asynchronous data transfer is also called as Handshaking.

37. Define Baud rate (Nov/Dec 2004,2018)

The number of bits transmitted per second is called baud rate. The standard baud rates are 75, 110, 150, 300, 600, 1100, 2400, 9600 and 19200.

38. How do you initiate DMA with HOLD and HLDA?

In order to transfer bulk amount of data between memory and I/O device, I/O device sends request to DMA and then DMA sends HOLD request to microprocessor. Microprocessor leaves bus control to other and sends HLDA acknowledge to DMA

39. What is TXD?

TXD – Transmitter Data Output.

This output pin carries serial stream of the transmitted data bits along with other information like star bit, stop bits and priority bit.

40. Compare parallel data transfer and serial data transfer.

S.no	Parallel Data Transfer	Serial Data Transfer
1	8 bits of data is transferred at a time , in case of 8085 interfacing	one bits of data is transferred at a time
2	9 lines required to be connected between 2 points	Only 2 lines required to be connected
3	It is mainly used in small distance only	It is mostly used in long distance
4	Data transfer is fast	Data transfer is slow

41. What is TXD?

TXD – Transmitter Data Output.

This output pin carries serial stream of the transmitted data bits along with other information like star bit, stop bits and priority bit.

42. What is RXD?

RXD – Receive Data Input

This input of 8251 A receives a composite steam of the data to be received by 8251 A.

43. What is the function of gate signal in 8254 timer? (May/June 2007)

The gate signal in 8254 is used as the gate input of counters. CLKO, CLK1 gate signals are given to counter 0, counter 1 and counter 2 respectively.

44. Draw the Status word format for 8254.

OUT	NULL	RW1	RW0	M2	M1	M0	BCD

45. Name the six modes of operations of an 8253 programmable interval timer.

What are the modes of operation used in 8253?/ [NOV/DEC 2006]

List the six modes of timer. (AU May 2012,2015,2018)

Each of the three counters of 8253 can be operated in one of the following six modes of operation.

- Mode 0 (Interrupt of terminal count)
- Mode 1 (Programmable monoshot/ hardware triggerable one-shot)
- Mode 2 (Rate generator)
- Mode 3 (Square wave generator)
- Mode 4 (Software triggered strobe)
- Mode 5 (Hardware triggered strobe)

46. What are the modes used in display modes?

Left Entry mode

In the left entry mode, the data is entered from the left side of the display unit.

Right Entry mode

In the right entry mode, the first entry to the displayed is entered on the right most display.

47. What is the difference between two key lockout and N-key rollover modes in 8279? (April/May 2005)

Two-key Lockout mode:
If two keys are depressed within the debounce cycle, it is a simultaneous depression. Neither key will be recognized until one of the key is released. The final key released will be recognized and entered.
N-Key Rollover mode:
In this mode, each key depression is treated independently. If simultaneous depression occurs, then keys are recognized and entered according to the order the keyboard scan found them.

48. What are the modes used in keyboard modes?

- Scanned keyboard mode with 2 key Lockout
- Scanned keyboard with N-key Rollover.
- Scanned keyboard special Error Mode.
- Sensor Matrix Mode

49. List the functions performed by 8279.(April/May 2005)

1. Keyboard Scanning
2. Key debouncing
3. Keycode generation
4. Informing the key entry to CPU
5. Storing display codes
6. Output display codes to LEDs
7. Display refreshing

50. What is key bouncing? (April/May2007, 2008)

Mechanical switches are used as keys in most of the keyboards. When a key is pressed the contact bounce back and forth and settle down only after a small time delay (about 20ms). Even though key is actuated once, it will appear to have been actuated several times. This problem is called key Bouncing.

51. What is meant by time multiplexed LED display? (Nov/Dec 2005)

In time multiplexed LED display, at a time only one LED displays data while other LEDs remain in OFF condition. But within few milliseconds, next LED is turned on while all others are in OFF condition. This is repeated continuously so that all LEDs seem to display data simultaneously.

52. Define scan counter?[NOV/DEC 2011]

The scan counter has two modes to scan the key matrix and refresh the display. In the encoded mode, the counter provides binary count that is to be externally decoded to provide the scan lines for keyboard and display. In the decoded scan mode, the counter internally decodes the least significant 2 bits and provides a decoded 1 out of 4 scan on SL0-SL3. The keyboard and display both are in the same mode at a time.

53. Give the different types of command words used in 8259?

The command words of 8259 A are classified in two groups

Initialization command words (ICWs)

Operation command words (OCWs)

54. Give the operating modes of 8259?

(a) Fully Nested Mode
(b) End of Interrupt (EOI)
(c) Automatic Rotation
(d) Automatic EOI Mode
(e) Specific Rotation
(f) Special Mask Mode
(g) Edge and level Triggered Mode
(h) Reading 8259 Status
(i) Poll command
(j) Special Fully Nested Mode
(k) Buffered mode
(l) Cascade mode

55. State the use of cascading signals of 8259 programmable interrupt control? [APR / MAY 2011].

8259 can be cascaded with other 8259's order to expand the interrupt handling capacity to 64 levels. [Master – Slave modes]

56. What is the usage of IRR (Interrupt Request Register)? (Nov/Dec 2008)

IRR is the register available in programmable interrupt controller (8259). It is used to store all the interrupt levels which are requesting service. IRR is cascaded with In-service register (ISR).

57. What signals are required between a 8085 processor and interrupt controller for interrupt driven data transfer? [NOV / DEC 2010]

Interrupt signal Eg. RST 7.5 & AD0 – AD7

58. Name the three modes used by the DMA processor to transfer data? [NOV/DEC 2006]

- Signal transfer mode (cycling stealing mode)
- Block transfer mode
- Demand transfer mode

59. What are the Control signals used for DMA operation

HOLD & HDLA

60. What is meant by DMA data transfer? (May/June 2009, Nov/Dec 2004,2016)

DMA stands for Direct Memory Access. In order to transfer bulk amount of data between memory and I/O device without the involvement of CPU, this technique is used.

61. Why is each channel in DMA controller restricted to 19Kbytes of data transfer? [APR / MAY 2010].

Mostly we use 8085 and 8086 microprocessor to interface with DMA controller.

62. What is meant by DMA operation? State its advantages.(Nov/Dec 2005,2017)

What is DMA? (AU Nov 2011)

DMA stands for Direct Memory Access. In order to transfer bulk amount of data between memory and I/O device without the involvement of CPU, this technique is used. The advantage of DMA is faster data transfer.

PART-B

1. Explain in detail about Memory Interfacing and I/O interfacing of 8086.
2. Describe the internal block diagram of 8255 (December 2010) (or)
   Parallel communication interface (8255) **(May 2018,2017)**
3. Explain in detail about Serial Communication Interface **(Dec 2016,May 2019)**
4. Draw the block diagram of 8279 Keyboard/Display controller and explain how to interface the Hex Key Pad and 7-segment LEDs using 8279. (April 2010)
5. Draw the functional block diagram of 8254 timer and explain the different modes of operation. (April 2010)(Nov/Dec-2013)
6. Discuss in detail about Programming and interfacing 8253
7. Explain in detail about Direct Memory Access (DMA Controller 8257) .(Nov/Dec 2017 ,2018) **May 2018**
8. Write in detail about Analog to digital conversion (ADC). .(Nov/Dec 2017, 2018)
9. Explain in detail about Interfacing Digital to Analog Converters. .(Nov/Dec 2018)
10. Draw the block diagram of 8259A and explain how to program 8259A (April 2010). **(**May 2019, Dec 2016)
11. Explain in detail Programmable Interval Timer: 8254
12. Explain in detail about Traffic light Control
13. Discuss the following in detail
    (i). Interfacing LED with 8086 (**May 2018,19)**
    (ii) Interfacing LED with 8086
    (iii) Keyboard interface **(May 2017)**
14. Explain in detail about alarm controller.

UNIT-IV (MICROCONTROLLER)

1. What is mean by microcontroller?[APR/MAY 2011]

Microcontroller is a device that includes microprocessor, memory and I/O port lines on a single chip, fabricated using VLSI technology.

2. What is Microcontroller and Microcomputer?[APRIL/MAY/ 2011]

Microcontroller is a device that includes microprocessor, memory and I/O signal lines on a single chip. Microcomputer is a computer that is designed using microprocessor as its CPU. It includes microprocessor, memory and I/O.

3. Compare Microprocessor and Microcontroller.[May 2009, NOV 2006, NOV 2011]

What are the differences between a microprocessor and a microcontroller? (May 2007, Nov 2011,2018)

Sl.No	Microprocessor	Microcontroller
1.	A microprocessor is a general purpose device which is called a CPU.	A microcontroller is a dedicated chip which is also called single chip computer.
2.	A microprocessor does not contain on chip I/O Ports, Timers, Memories etc.	A microcontroller includes RAM, ROM, serial and parallel interface, timers, interrupt circuitry in a single chip.
3.	Microprocessor is used as the CPU in microcomputer system.	Microcontroller is used to perform control-oriented applications.
4.	Microprocessor instructions are nibble or byte addressable	Microcontroller instructions are both bit addressable as well as byte addressable.

4. List the features of 8051 microcontroller.[MAY 2007][NOV 2007, NOV 2011]

The 8051 is an 8-bit Microcontroller:

- ✓ The CPU can work on only 8 bits of data at a time
- ✓ The 8051 has
- 128 bytes of RAM
- 4K bytes of on-chip ROM
- Two timers

5. List the applications of microcontroller. [MAY/JUNE 2009]

Microcontroller is used various control applications**:**

- Fire detection in Building.
- Industrial control(process control)
- Motor speed control (stepper motor control)
- Peripheral devices(printer)
- Stand alone devices(color Xerox machine)
- Automobile applications(power steering)
- Home applications(washing machine, AC)

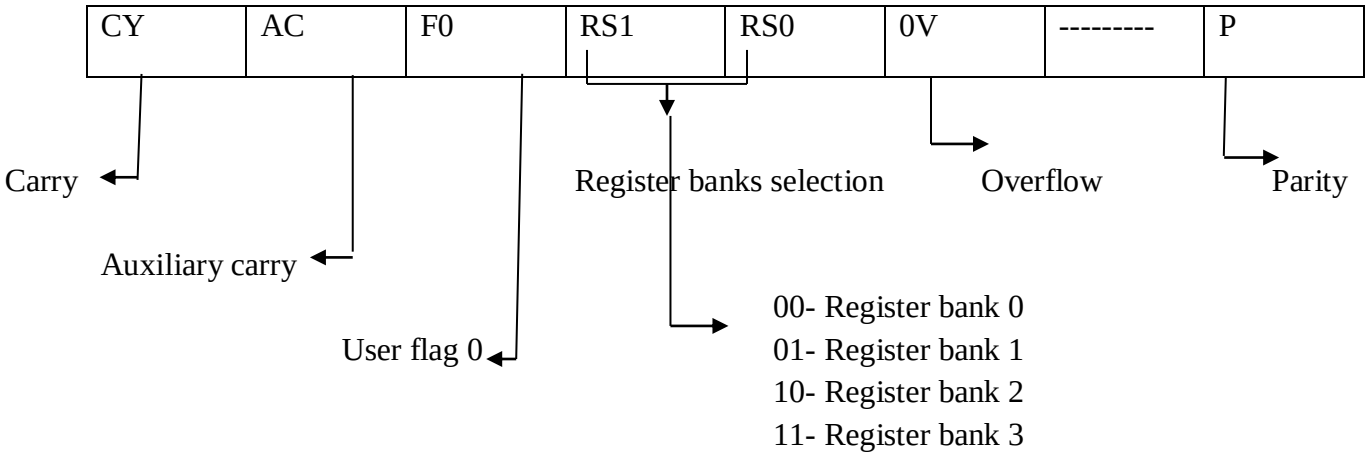
6. Mention the different operand types used in 8051. (NOV 2012)

Register operand, immediate operand, Direct operand, Direct – offset operand and Indirect operand.

7. What are the addressing modes supported by 8051? [May 2010, May 2009, MAY 2008, NOV2011]What are the different ways of operand addressing in 8051? (May 2016,NOV/Dec 2018)

1. Immediate addressing mode
2. Direct Addressing mode
3. Register addressing mode
4. Register indirect addressing mode
5. Indexed addressing mode

8. **Draw the format of PSW of 8051.(May 2015)**



9. **State the function of RS1 and RS0 bits in the flag register of Intel 8051 microcontroller.[NOV2011]**

   How do you select the register bank in 8051 micro-controller? (May 2010, NOV 2008, May 2008, May 2016)

   Mention the number of register banks and their addresses in 8051. (NOV 2015)

   ✓ RS1 & RS0 are used to indicate which bank currently in use.

RS1	RS0	Register bank Selection	Addresses of Register banks
0	0	Register Bank 0	00H to 07H
0	1	Register Bank 1	08H to 0FH
1	0	Register Bank 2	10H to 17H
1	1	Register Bank 3	18H to 1FH

   RS1, RS0 – Register bank select bits

10. **In the program status word of 8051, the bits RS0 and RS1 are 1 and 0, then which register bank is selected for operation? (AU May 2013) (May 2019)**

Register Bank 1is selected.

11. **Explain the 16-bit registers DPTR of 8051.[MAY/JUNE 2007]**

What is the use of DPTR? (May2009)

DPTR: DPTR stands for data pointer. DPTR consists of a high byte (DPH) and a low byte (DPL). Its function is to hold a 16-bit address.

It may be manipulated as a 16-bit data register or as two independent 8-bit registers. It serves as a base register in external data transfer.

12. **What are the advantages of microcontroller over microprocessor?**

    What are the advantages of using a microcontroller in place of a microprocessor? (AU May 2011 MAY 2008)

- The overall system cost is low, as the peripherals are integrated in a single chip.
- The size is very small.
- The system is easy to troubleshoot and maintain.
- The system is more reliable.

13. Define XTAL1 and XTAL2. [MAY/JUNE 2009]

- These two pins are connected to Quartz crystal oscillator which runs the on-chip oscillator.
- If use a source other than the crystal oscillator, it will be connected to XTAL1 and XTAL2 is left unconnected.

14. Name the special functions registers available in 8051.[MAY2007, NOV 2007, May 2008, May 2010]

- Accumulator
- B Register
- Program Status Word
- Stack Pointer
- Data Pointer
- Port 0, Port 1, Port 2 & Port 3
- Interrupt priority control register
- Interrupt enable control register

15. What is the importance of special functions registers available in 8051 microcontroller?

- ✓ The 8051 operations that do not use the internal 128 byte RAM address from 00H to 7FH.
- ✓ 128 byte RAM locations used by a group of special internal registers.
- ✓ SRFs (special function registers), which may be addressed like internal RAM.

16. How is stack implemented in 8051? (or) What is stack pointer and write the stack level of 8051? (NOV 2007)

- ✓ The 8051 LIFO: Stack can reside anywhere in the internal RAM.
- ✓ It has 8 bit stack pointer to indicate the stop of the stack using PUSH and POP instructions.
- ✓ During PUSH the SP is incriminated by one and POP the SP is decremented by one.

17. What is the use of RET and RETI instruction in 8051?

RET – Return to subroutine
Used to return from a subroutine previously entered by CALL instructions
RET – Return to interrupt
Used at the end of interrupt service routine(ISR)

18. List the 8051 instructions that affect the flags. [NOV/DEC 2007]

ADD, ADDC, DIV, MUL and SUB B

19. List the 8051 instructions that always clear the carry flag.

CLR C, DIV, MUL

20. Give the functions of the EA pin of 8051. (NOV 2016)

How the processor 8051 does know whether on-chip ROM or external program memory is used? (May 2014)

EA: EA stands for External Access.

- ✓ This pin is an active low pin. This pin should not be left unconnected.
- ✓ This pin is connected to ground when microcontroller is accessing the program code stored in the external memory.
- ✓ This pin is connected to Vcc when it is accessing the program code in the on chip memory.

21. Give the function of the SP register of 8051. [NOV/DEC2011] (May 2018)

SP: SP stands for stack pointer.

- ✓ SP is an 8-bit wide register.
- ✓ It is incremented before data is stored during PUSH and CALL instructions.
- ✓ The stack pointer is initialized to 07H after a reset.

22. What are the functions of the following signals of 8051? $\overline{\text{ALE}}$/PROG, PSEN. (AU Nov 2010)

ALE (Address Latch Enable):

- ✓ This is an output pin and is active high.
- ✓ When connecting an 8051 to external memory, Port 0 provides both address and data.
- ✓ If ALE=0, Port 0 (D_0-D_7). If ALE=1,it has (A_0-A_7).

PSEN (Program Store Enable):

- ✓ This is an output pin.
- ✓ In 8051-based system in which an external ROM holds the program code, this pin is connected to the OE pin of the ROM.

23. Give the alternate functions for the port pins of port 3. [APRIL/MAY 2011]

Which port used as multifunction port? List the signals. (April 2017)

Port 3 is used as multifunction port and its signals are

- ✓ RD – Read data control output
- ✓ WR – Write data control output
- ✓ T1 – Timer / Counter1 external input or test pin
- ✓ T0 – Timer / Counter0 external input or test pin
- ✓ INT1 – Interrupt 1 input pin
- ✓ INT0 – Interrupt 0 input pin
- ✓ TXD – Transmit data pin for serial port in UART mode
- ✓ RXD – Receive data pin for serial port in UART mode

24. List the ports available in 8051. (or)

How many ports are bit addressable in 8051? (NOV 2011, NOV 2009)

- ✓ The four ports are P0 (Port 0), P1 (Port1), P2 (Port 2) and P3 (Port3).
- ✓ Four ports are bit addressable.

25. How does the status of EA pin affect the access to internal and external program memory?

- ✓ If EA=0, 8051 can access the external program memory.
- ✓ EA=1, accesses the internal program memory.

26. What is the size of the on-chip program memory and on-chip data memory of 8051 microcontroller? (AU May 2012, NOV 2011)

- ✓ The size of the on-chip program memory of 8051 microcontroller : 4K
- ✓ The size of the on-chip data memory of 8051 microcontroller : 128 bytes

27. What is the difference between timer and counter operations in 8051?

- ✓ The timer, counts the internal clock pulses whose frequency is $1/12^{th}$ of oscillator frequency.
- ✓ The counter, counts the external clock pulses which are given through T0 pin and T1 pin of 8051.

28. Define watch dog timer.

- ✓ Watch dog timer is a dedicated timer to take care of system malfunction.
- ✓ It can be used to reset the controller during software malfunction.

29. What is the function of TMOD register?

- ✓ TMOD (timer mode) register is used to set the various timer operation modes.
- ✓ TMOD is dedicated to the two timers (Timer 0 and Timer 1) .

30. If a 12 MHz crystal is connected with 8051, how much is the time taken for the count in timer 0 to get incremented by one?

Baud rate $= \frac{\text{oscillator frequency}}{12}$

$= \frac{12\text{MHz}}{12} = 1\text{MHz}$

T=1/f=1/1MHz = 1 micro sec

31. What is the time duration for one state and one machine cycle if a 6MHz crystal is connected to 8051?

Clock frequency=6MHz/12=0.5MHz

One T state = 1/clock frequency =1/0.5MHz =2 micro sec

The time taken to execute a machine cycle is 12 clock periods.

32. What happens in power down mode of 8051 micro controller? (May 2016)

- ✓ The memory locations of power down RAM can be maintained through a separate small battery backup supply.
- ✓ So that the content of these RAM can be preserved during power failure conditions.

33. Define baud rate. (May 2016)

- ✓ Baud rate is used to indicate the rate at which data is being transferred.
- ✓ Baud rate = 1/Time for a bit cell

34. Give the register IE format of 8051. (or)
Mention the use of interrupt enable register in 8051. (May 2009)

EA	—	ET2	ES	ET1	EX1	ET0	EX0

- ✓ EA – Enable all control bit
- ✓ ET2 – Timer w interrupt enable bit
- ✓ ES – Enable serial port control bit
- ✓ ET1 – Enable Timer 1 control bit
- ✓ EX1 – Enable external interrupt 1 control bit
- ✓ ET0 – Enable Timer control bit
- ✓ EX0 – Enable external interrupt control bit

35. Name the interrupt sources of 8051 for which the priority levels are highest, lowest respectively. (Dec 2017)

1) IEO — highest priority
2) TFO
3) IE1
4) TF1
5) Serial RI or TI — lowest

36. What is the function of IP register in 8051? (or)What register keeps track of interrupt priority in the 8051? Explain. (NOV 2009)

The IP register is used to set high priority to one or more interrupts in 8051.

----	----	---	PS	PT1	PX1	PT0	PX0

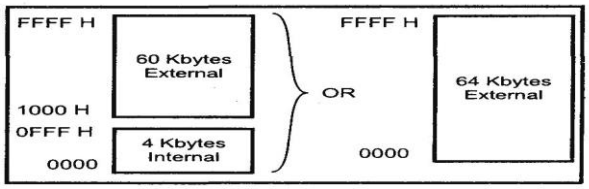
- ✓ Setting a bit, makes the corresponding interrupt to have high priority.
- ✓ Clearing a bit, makes the corresponding interrupt to low priority.

37. Name the five interrupt sources of 8051. [May 2010, NOV 2009, MAY2007, MAY 2008] What is the hardware and software interrupts of 8051? Mention its vector addresses. (NOV 2011)

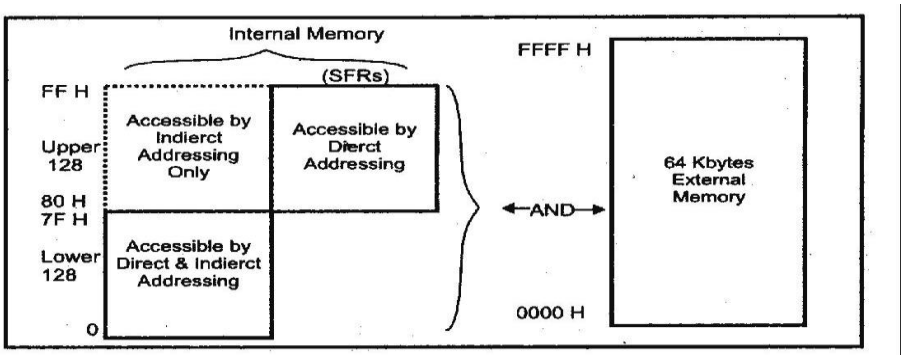
The interrupts with vector address are:

- External interrupt 0: IE0: 0003H
- Timer interrupt 0: TF0: 000BH
- External interrupt 1: IE0: 0013H
- Timer interrupt 0: TF1: 001BH
- Serial interrupt
- Receive interrupt RI: 0023H
- Transmit interrupt TI:0023H

38. Draw the program memory organization in 8051.



39. Draw the data memory organization in 8051.



40. Define Program Counter.

- ✓ Program counter (PC) is a 16 bit register.
- ✓ It holds the 16-bit address of the instruction to be executed by the processor.
- ✓ PC is automatically incremented after every fetch of instruction byte from the memory.

41. Why all pins of a port is loaded with value "FF" before using it?

- ✓ All ports of 8051 are configured by default as Output port.
- ✓ To make it configured as Input Port, all pins of a port are loaded with value "FF" i.e., 1111 1111.

42. Justify why the crystal oscillator frequency in 8051 is chosen as 11.0592Mhz.

- ✓ Only XTAL (Crystal Oscillator) of 11.0592 MHz can provide such standard baud rates 4800, 9600, etc., after scaling down by 12, 32 at UART.

42. List the modes of Timer in 8051. (NOV 2008)

The modes of timer in 8051 are chosen with M0 & M1 bits in TMOD register. The different modes of timer are as follows.

M1	M0	Mode	Description of Timer mode
0	0	0	13 bit timer
0	1	1	16-bit timer
1	0	2	8-bit timer with auto reload
1	1	3	Split timer

43. What is the significance of C/T bit in TMOD register of 8051?

- ✓ The C/T bit in the TMOD register is a selector bit for the type of operation.
- ✓ HIGH in that bit indicates Counter operation and LOW in that bit indicates Timer operation.

44. What is the significance of TRx bit in TCON register of 8051? (May 2015)

TRx bit in the TCON register is used to Start / Stop the timer register for both timer and counter operation, by setting that bit with value '1' / '0' respectively.

45. What are the modes of asynchronous serial communication in 8051? (NOV 2008,2015)

- ✓ The mode of serial communication is decided by two bits SM0 & SM1 in SCON register.
- ✓ The detail of the various modes is given below.

SM1	SM0	Mode	Serial Mode Description	Baud rate
0	0	0	8-bit Shift register	F_{Osc} / 12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	F_{Osc} / 32 or 64
1	1	3	9-bit UART	Variable

46. Illustrate the CJNE instruction. (April 2017)

Compare and Jump if Not Equal – CJNE

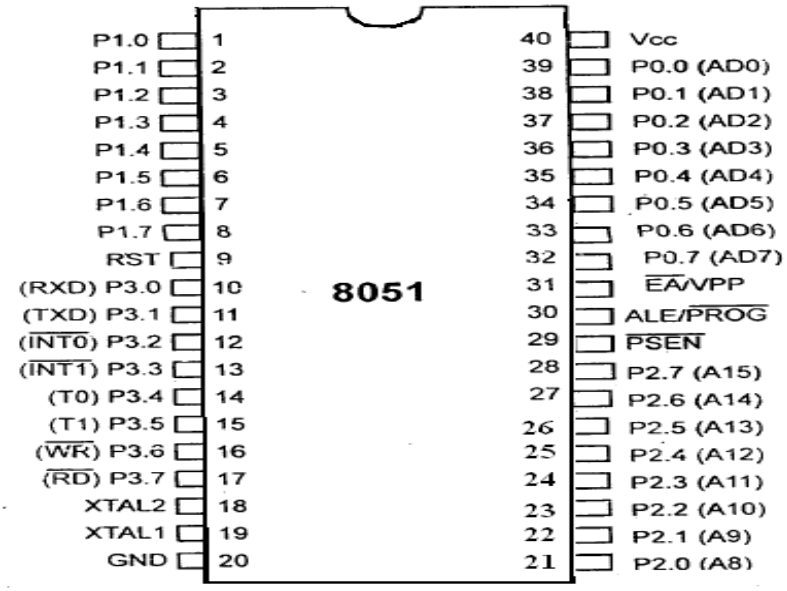
Compare the magnitude of the two operands and jump if they are not equal.

The values are considered to be unsigned.

The Carry flag is set / cleared appropriately.

Example: CJNE A, direct, rel

47. Draw the pin diagram of 8051. (NOV 2016)(May 2018)



48. What is jump range? (NOV 2015)
What is the difference between AJMP and LJMP instruction? (May 2014)

Jump Instruction	Meaning	Jump Range
SJMP	Short jump	256B
AJMP	Absolute jump	2KB
LJMP	Long jump	64KB

- AJMP and LJMP instructions are transfer program control to the specified vector address.
- Program control transfer ranges are 2KB for AJMP and 64KB for LJMP.

49. What are special function registers used for port operation in 8051? (May 2012)
P0, P1, P2 and P3 SFRs used for port operation.

50. What is need for bitwise instructions in microcontroller? (May 2012)
Bitwise instructions allow manipulating the individual bits of bit addressable registers and memory locations as well as the CY flag.

51. What are on-chip resources? List those available in the 8051 microcontroller. (NOV 2010)
When various resources available inside of chip is known as on-chip resources.
On-chip resources available in 8051 are RAM, ROM, Timer, Interrupts, serial ports and parallel ports.

52. A given 8051 chip has a speed of 16MHz. What is the range of frequency that can be applied to the XTAL1 and XTAL2 pins? (NOV 2009)
16MHz frequency can be applied to the XTAL1 and XTAL2 pins.

53. How do you calculate baud rate for serial communication for 8051? (NOV 2007, MAY 2013,2015)
8051 divides the crystal frequency by 12 to get machine cycle frequency.
8051 UART circuitry divides the machine cycle frequency by 32.
Timer 1 is used to set baud rate using TH1 register

Baud rate	TH1 (decimal)	TH1(Hex)
9600	-3	FD
4800	-6	FA
2400	-12	F4
1200	-24	E8

54. Why it is necessary to have external pull up for port 0 in 8051?[November 2014]

- ✓ When logic -1 is loaded to the latch.
- ✓ This causes port 0 to float to high impedance state and it gets connected to the Pin read buffer.
- ✓ An external pull up resistor is required to supply a high output.

PART-B

1. Draw the architectural block diagram of 8051 microcontroller and explain. (NOV 2011, MAY 2010, NOV 2009, NOV2008, May 2008, MAY 2007, MAY 2006, NOV 2016 ,2017, May 2016,2017)

2. Give PSW of 8051 and describe the use of each bit in PSW. (NOV 2015,2016)

3. Explain in detail the internal memory organization of 8051 microcontroller (NOV 2014, May 2012, NOV 2011, NOV 2010, May 2010, MAY 2009, NOV 2008, NOV 2007)

4. Write the available special function registers in 8051. Explain each register with its format and functions. (April 2017, NOV 2015) .(Nov/Dec 2016, 2018) **(May 2018,2019)**

5. What are the I/O ports available in 8051 and explain? (MAY 2014, NOV 2012, MAY2010, NOV2009,2017 ,2018)
   Enumerate about the ports available in 8051. (MAY 2014)
   Explain parallel port architecture of 8051 microcontroller. (NOV 2012)
   Explain each PORT circuitry available in 8051. (NOV 2007)
6. Explain interrupt structure of 8051 microcontroller. (NOV 2011, MAY 2009)
7. Explain in detail the timer of 8051 and their associated registers. (NOV 2009, MAY2009)
   How are the timers of 8051 used to produce time delay in timer mode? (NOV 2011)
8. Explain Pin details of 8051 microcontroller. (MAY 2006)

   Describe the functions of the following signals in 8051. RST, EA, PSEN and ALE. (NOV 2015)

9. Explain different types addressing modes of 8051 microcontroller. (NOV 2008, NOV 2015,16, April 2017,18,19)
10. Discuss in detail the 8051 instruction set. (NOV 2008)

11. Briefly explain the data transfer instructions available in 8051 microcontroller. (NOV 2014)

12. With example, explain branching instructions in 8051 microcontroller. (May 2010, NOV 2012)

13. Explain the working of program control transfer instructions of 8051. (May 2012)

14. Using timers in 8051 write a program to generate square wave 100ms, 50% duty cycle. (NOV 2014, May 2016, May 2012)

15. Write an 8051 ALP to multiply the given number 48H and 30H. (April 2017) **(May 2018)**

16. Write a program to add two 16 bit numbers. The numbers are 8C8D and 8D8C. Place the sum in R7 and R6. R6 should have the lower byte. (NOV 2010)

UNIT V (INTERFACING MICROCONTROLLER)

1. What are the registers used in timer programming of 8051?

- Timer1 (TH1,TL1)
- Timer0 (TH0.TL0)
- TMOD
- TCON

2. What are the various modes of 8051 timers? (NOV 2016)(Nov/Dec 2018) (May 2019)

The 4 modes available in timers are

S.No	M0	M1	Mode	Operation
1	0	0	Mode 0	**13-bit Timer mode.** 8-bit Timer/counter THx with TLx as 5-bit prescaler
2	0	1	Mode 1	**16-bit Timer mode**.16-bit timer /counter THx and TLx are cascaded. There is no presacler
3	1	0	Mode 2	**8-bit auto reload.** 8-bit auto reload timer/counter. THx holds a value which is to be reloaded TLx each time it overflows
4	1	1	Mode 3	**Split timer mode**

3. What are the methods used for serial communication?

- **Synchronous** method transfers a block of data (characters) at a time.
- **Asynchronous** method transfers a single byte at a time. Each character is placed between start an stop bits.

4. What is meant by framing?

In asynchronous serial data transmission, each character is placed between start and stop bits. This is called framing.

5. What is called baud-rate?

The number of bits transmitted per second in serial data communication is called bps(bits /second) or baud rate.

6. What is called RS232?

RS232 is a serial interfacing standard set by Electronics industries association to allow compatibility among data communication equipment.

7. List the handshake signals of serial communication.(Dec 2017)

- DTR – data terminal ready
- DSR – Data set ready
- RTS – Request to send
- CTS – clear to send

- DCD- data carrier detect
- RI –Ring indicator

8. What is the difference between timer and counter? (May 2007)

SI. No	Timer	counter
1.	Timer is used to generate a time delay	counters are used to count events happening outside the microcontroller
2.	Then C/T = 0, the timer is used as a timer a get its pulses from crystal oscillator inside t 8051	When C/T = 1, the timer is used as a counter and gets its pulses from outside the 8051
3.	The timer counts the internal clock pulses whose frequency is $1/12^{th}$ of oscillator frequenc	The counter counts the internal clock pulses which is given through either T0 pin and T1 pin of 8051.

9. What is the function of MAX 232?

MAX 232 is commonly referred as a line driver which is used as a voltage, converters to convert the TTL logic levels (0 and 1) to the RS232 voltage levels (+3V to +25V and -3V to -25V) and vice-versa.

10. What are the two ways to increase the baud rate more than 9600 in 8051?

There are two ways to increase the baud rate of data transfer in the 8051

- Use a high frequency crystal
- Change the SMOD bit in the PCON register

If SMOD = 1, the baud-rate is doubled.

11. What is an interrupt?

An interrupt is an external or internal event that interrupts the microcontroller to inform it that a device needs its service.

12. What is the difference to polling and interrupt method? (NOV 2015)

Polling	Interrupt
1. Polling can monitor the status of several devices and serve each of them as certain conditions are met 2. The polling method is not efficient, since it wastes much of the microcontroller's time by polling devices that do not need service	1.Upon receiving an interrupt signal, the microcontroller interrupts whatever it is doing and serves the device 2. The program which is associated with the interrupt is called the interrupt service routine (ISR) or interrupt handler

13. What is meant by interrupt vector table?

The group of memory locations set aside to hold the addresses of ISRs is called interrupt vector table.

14. What are the steps involved in executing interrupt?

1. It finishes the instruction it is executing and saves the address of the next instruction (PC) on the stack
2. It also saves the current status of all the interrupts internally (i.e: not on the stack)
3. It jumps to a fixed location in memory, called the interrupt vector table, that holds the address of the ISR.
4. The microcontroller gets the address of the ISR from the interrupt vector table and jumps to it.
5. Upon executing the RETI instruction, the microcontroller returns to the place where it was interrupted.

15. What are the possible interrupts of 8051?

- Reset – power-up reset
- Two interrupts are set aside for the timers:
  one for timer 0 and one for timer 1.
- Two interrupts are set aside for hardware external interrupts
  P3.2 and P3.3 are for the external hardware interrupts INT0 (or EX1), and INT1 (or EX2)
- Serial communication has a single interrupt that belongs to both receive and transfer.

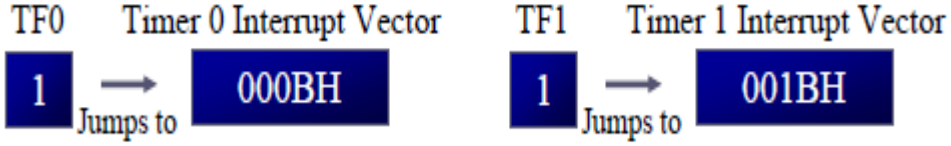
16. What is the purpose of IE (interrupt Enable)Register?

EA	—	ET2	ES	ET1	EX1	ET0	EX0

- EA : Global enable/disable. To enable the interrupts, this bit must be set high.
- --- : Undefined-reserved for future use.
- ET2 : Enable /disable Timer 2 overflow interrupt.
- ES : Enable/disable Serial port interrupts.
- ET1 : Enable /disable Timer 1 overflow interrupt.
- EX1 : Enable/disable External interrupt1.
- ET0 : Enable /disable Timer 0 overflow interrupt.
- EX0 : Enable/disable External interrupt0

17. How timer interrupts are generated in 8051?

If the timer interrupt in the IE register is enabled, whenever the timer rolls over, TF is raised. The microcontroller is interrupted in whatever it is doing and jumps to the interrupt vector table to service the ISR



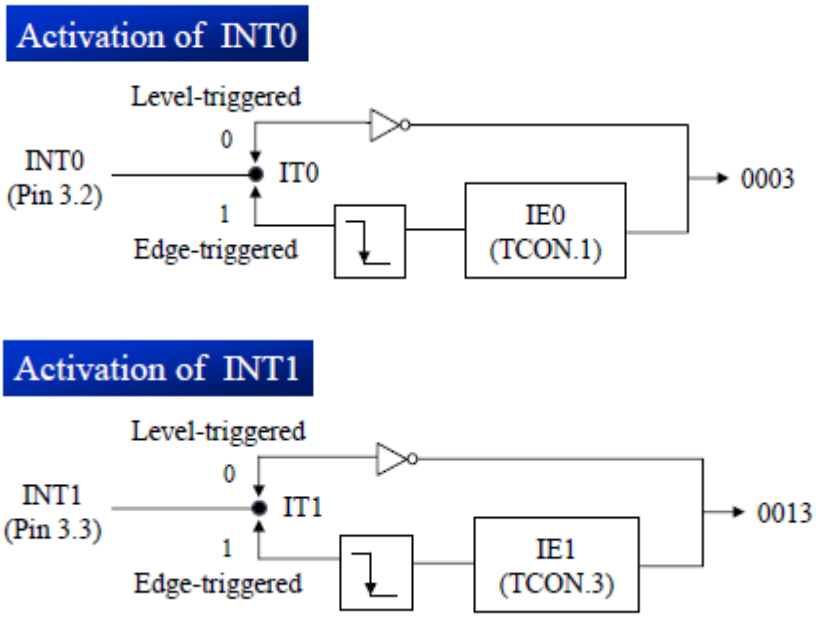
18. What are the external H/W interrupts available in 8051?

Pin 12 (P3.2) and pin 13 (P3.3) of the 8051, designated as INT0 and INT1, are used as external hardware interrupts.

The interrupt vector table locations 0003H and 0013H are set aside for INT0 and INT1.

There are two activation levels for the external hardware interrupts

- Level trigged
- Edge trigged



21. What is the difference between RET and RETI instruction?(April 2008)

RET	RET1
1. Return to caller 2. After finishing execution of the Subroutine ,the instruction RET transfers control back to the caller 3. Every subroutine needs RET as the last Instruction.	1. Return from interrupt 2. Upon executing the RETI instruction, the micro-controller returns to the place where it interrupted. 3. Every interrupt service subroutine needs RETI the last instruction.

22. What are the flags used for interrupt?

- Timer 1 overflow flag (TF1)
- Timer 0 overflow flag (TF0)
- External interrupt 1 edge flag (IE1)
- External interrupt 0 edge flag (IE0)
- Serial communication interrupt flag.(RI or TI)

23. List the 8051 interrupts with its priority. (April 2017, 2018)

- ✓ Upon reset, the interrupts have the following priority from top to down. The interrupt with the highest PRIORITY gets serviced first.

1. External interrupt 0 (INT0)
2. Timer interrupt0 (TF0)
3. External interrupt 1 (INT1)
4. Timer interrupt1 (TF1)
5. Serial communication (RI+TI)

24. What are the default values of the registers in 8051?

Register	Reset Value
PC	0000
DPTR	0000
ACC	00
PSW	00
SP	07
B	00
P0-P3	FF

25. What are the source of interrupts in 8051?(Dec 2009)

- Reset
- Timer o
- Timer1
- External interrupt INT0
- External Interrupt INT1
- Serial communication transmit and receive interrupt.

26. What is the use of SBUF register? (NOV 2009, May 2006,2015)

SBUF is an 8-bit register used for serial communication.

At transmitter section

For a byte data to be transferred via the TxD line, it must be placed in the SBUF register.

At receiver section

SBUF holds the byte of data when it is received by 8051 RxD line.

27. What is the use of SCON register?

SCON is an 8-bit register used to program the start bit, stop bit, and data bits of data framing, among other things.

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Bit Number	Bit Mnemonic	Description
SCON.7	SM0	Serial port mode specifier
SCON.6	SM1	Serial port mode specifier
SCON.5	SM2	Used for multiprocessor communication
SCON.4	REN	Set/Cleared by software to enable/disable reception
SCON.3	TB8	Not widely used
SCON.2	RB8	Not widely used
SCON.1	TI	Transmit interrupt flag. Set by hardware at begin of the stop bit mode 1. And cleared by software
SCON.0	RI	Receive interrupt flag. Set by hardware at begin of the stop bit mode 1. And cleared by software

28. What is the importance of RI and TI flags?

- When 8051 finishes the transfer of 8-bit character. It raises TI flag to indicate that it is ready to Transfer another byte. **TI** bit is raised at the beginning of the stop bit.
- It raises the **RI** flag bit to indicate that a byte has been received and should be picked up before it is lost. RI is raised halfway through the stop bit.

29. Which register is used to set the data size and other framing information such as the stop bit?

SCON register

30. What is the role of REN bit in the SCON register?

REN (receive enable). It is a bit-addressable register.

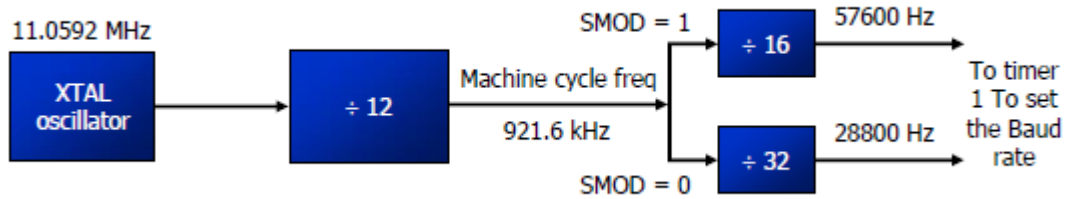
When it is high, it allows 8051 to receive data on RxD pin

If low, the receiver is disabled.

31. What is the use of PCON register?

SMOD	--	--	--	GF1	GF0	PD	IDL

- PCON register is an 8-bit register
- When 8051 is powered up, SMOD is zero.
- We can set it to high by software and thereby double the baud rate.
- GF1, GF0: General flag bits
- PD: Power down mode
- IDL: Ideal mode



32. What are the advantages of LCD over LED?(NOV/DEC 2018)

LCD is finding widespread use replacing LEDs because

- The declining prices of LCD
- The ability to display numbers, characters, and graphics
- Ease of programming for characters and graphics.

33. What is the difference between Vcc, VEE pin on the LCD?

- **Vss** ground
- **Vcc** +5v power supply
- **VEE** power supply to control contrast.

34. What is the need for ADC services?

ADCs (analog-to-digital converters) are widely used devices for data acquisition.

We need an analog-to-digital converter to translate the analog signals to digital numbers, so microcontroller can read them.

35. What is the need for D/A Converter?(Nov 2005)

The microcontroller can produce only digital signals. Analog signals are needed for controlling certain analog devices in many applications. The D/A converters are used for converting the digital signals into analog signals.

36. What is meant by transducer?

A physical quantity, like temperature, pressure, humidity, and velocity, etc., is converted to electrical (voltage, current)signals using a device called a transducer, or sensor.

37. Indicate the steps to detect the key pressed.

- To detect a pressed key, the microcontroller grounds all rows, then it reads the columns
- If the data read from columns is D3 – D0 = 1111, no key has been pressed and the process continues till key press is detected
- If one of the column bits has a zero, this means that a key press has occurred .

40. What is meant by stepper motor?

A stepper motor is a digital motor used to translate electrical pulses into mechanical movements.

It is used in disk drives, dot matrix printers and robotics for position control.

41. What is the purpose of TMOD register?

TMOD (timer mode) register is used to set the various timer operation modes. TMOD is dedicated to timers (Timer0 and Timer1). It can be considered to be two 4 bit registers. Each of which controls the action of the timers.

42. If a 12 MHz crystal is connected with 8051, how much is the timer taken for the count in timer 0 to get incremented by one?(dec 2005)

Baud rate = $\frac{Oscillator\_frequency}{12}$

f=12* 10^6/ 12 =1*10^6 Hz

Time taken T= $\frac{1}{f}$ =10^{-6} sec= 1 microsec

43. What is the time duration for one machine cycle if a 6 MHz crystal is connected to 8051?

Clock frequency= 6 MHz/12 = 0.5 MHZ

1 T state = 1/clock frequency= $\frac{1}{0.5MHz} = 2\mu s$

Time taken to execute a machine cycle is 2µs

44. What are the different types of ADC? (April 2008,Nov 2011)

The different types of ADC are successive approximation ADC, Counter type ADC & Flash type ADC.

45. Give steps to program 8051 for serial data transfer.

- The 8051 has a serial data communication circuit that uses register SBUF to hold the data.
- Register SCON controls data communication
- Register PCON controls data rates
- Pins RxD (P3.0) and TxD (P3.1) connect to the serial data network.

46. Mention any two application of ADC and DAC (May 2011)

The application of ADC and DAC includes

DC motors

Digital computers

47. Define access time of memory.

The speed of the memory chip is commonly referred to as its access time.

48. What is meant by ROM?

ROM is a type of memory that does not lose its contents when the power is turned off

ROM is also called nonvolatile memory. There are different types of read-only memories

- PROM
- EPROM
- EEPROM
- Flash EPROM

49.What is called RAM?

RAM memory is called volatile memory. Since cutting off the power to the IC will result in the loss of Data.Sometimes RAM is also referred to as RAWM (read and write memory).

There are three types of RAM

- Static RAM (SRAM)
- NV-RAM (nonvolatile RAM)
- Dynamic RAM (DRAM)

50. What are the steps to be followed during connection of an external memory? (May 2019)

- The data bus of the CPU is connected directly to the data pins of the memory chip.
- Control signals RD (read) and WR (memory write) from the CPU are connected to the OE (output enable) and WE (write enable) pins of the memory chip.
- In the case of the address buses, while the lower bits of the address from the CPU go directly to the memory chip address pins, the upper ones are used to activate the CS pin of the memory chip.

51. What is the significance of ALE signal in connecting external memory?

- For ALE = 0, and P0 is used as a data bus, sending data out or bringing data in
- Whenever the 8031/51 wants to use P0 as an address bus, it puts the addresses A0 – A7 on the P0 pins and activates ALE = 1.

52. What happens in power down mode of 8051 microcontroller (June 2009, May 2016)

The memory locations of power down RAM can be maintained through a separate small battery backup supply.

So that the content of these RAM can be preserved during power failure conditions**.**

53. What are the types of sensors used for interfacing? (Dec 2017,April 2017,2018)

Temperature sensor, water level sensor, IR sensor are used to interfacing.

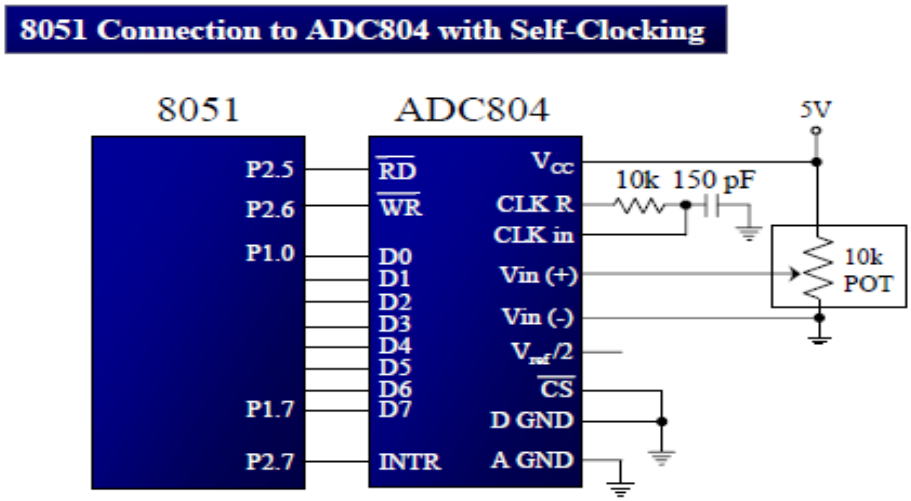
54. Write about the design steps involved in using microcontroller for stepper motor. (May 2014, May 2016)

- The stepper motor is connected with Microcontroller output port pins through a ULN2003 driver.
- The Microcontroller’s pin can provide a maximum of 1-2mA current.

- Place a driver, such as the ULN 2003/ULN2803or a power transistor between the Microcontroller and the coil to energize the stator.
- When the microcontroller is giving pulses to the stator windings, motor is rotated in clockwise or anticlockwise.

55. How is A/D converter interfaced with 8051? (NOV 2015)

- Analog input voltage (voltage range from 0V to 5V) is given to $V_{in(+)}$
- Converted digital output is given to 8051 through port 1.



56. List the SFRs involved in interrupt programming of 8051. (NOV 2014)

IE and IP registers involved in interrupt programming of 8051.

57. What is the use of PWM in motor control using microcontroller? (NOV 2012)

- PWM is used in motor control to provide various frequencies of the pulses to stator windings.
- It controls speed of the motor.

58. What is the significance of GATE bit in TMOD control register? (May 2007) (NOV/Dec 2018)

- ✓ This bit is used to start or stop the timers by hardware.
- ✓ When GATE= 1, the timers can be started / stopped by the external sources.
- ✓ When GATE= 0, the timers can be started or stopped by software instructions like SETB TR_X or CLR TR_X

59. What is the architecture followed by PIC?

PIC microcontrollers are based on advanced RISC architecture. RISC stands for Reduced Instruction Set Computing. In this architecture, the instruction set of hardware gets reduced which increases the execution rate (speed) of system. PIC microcontrollers follow Harvard architecture for internal data transfer.

60. Compare PIC and ARM microcontrollers.

Advanced RISC Machine, originally Acorn RISC Machine, is a family of reduced instruction set computing (RISC) architectures for computer processors, configured for various environments.

Arm Holdings develops the architecture and licenses it to other companies, who design their own products that implement one of those architectures—including systems-on-chips (SoC) and systems-on-modules (SoM) that incorporate memory, interfaces, radios, etc.

It also designs cores that implement this instruction set and licenses these designs to a number of companies that incorporate those core designs into their own products.
Processors that have a RISC architecture typically require fewer transistors than those with a complex instruction set computing (CISC) architecture (such as the x86 processors found in most personal computers), which improves cost, power consumption, and heat dissipation.

PIC microcontrollers are based on advanced RISC architecture. RISC stands for Reduced Instruction Set Computing. In this architecture, the instruction set of hardware gets reduced which increases the execution rate (speed) of system. PIC microcontrollers follow Harvard architecture for internal data transfer.

PART-B

1. Explain the different modes of operation of timers in 8051 in detail with its associated registers. (Or)

   Describe different modes of operation of timers /counters in 8051 with its associated registers. (NOV 2009,2017, MAY 2009. May 2007, May 2016) (Or)

   Draw and explain the functions of TCON and TMOD registers of 8051. (Dec 2008) (Or)

   Explain the on-chip timer modes of an 8051 Microcontroller. (April 2010, NOV 2016)

2. Explain the serial programming of 8051 with its associated registers. (May 2014, 2013,2017)(Or)

   Explain how to program for sending and receiving data serially using 8051 (April 2010, 2011) (Or)

   Explain 8051 serial port programming with examples. (May 2016, NOV 2012) (Or)

   Explain the serial modes of operation of 8051 microcontroller. (May 2007) (Or)

   Explain in detail the serial communication registers of the 8051. (NOV 2009)

   Write a program for the 8051 to transfer "YES" serially at 9600 baud, 8-bit data, 1 stop bit do this continuously. (May 2006) (**Dec 2017)**

   Write a program for the 8051 to receive bytes of data serially and put them in P1, set the baud rate at 4800, 8-bit data and 1 stop bit. (NOV 2016)

3. Explain how LCD is used to interface with 8051. (May 2007) (**May 2019)**
4. How does one interface a 16 × 2 LCD Display using 8051 Microcontroller? (May2009, May 2010)
5. With neat circuit diagram explain how a 4 x 4 keypad is interfaced with 8051 microcontroller and write 8051 ALP for keypad scanning. (May 2013, Nov 2015, NOV 2007)
6. Explain how to interface an 8-bit ADC with 8051 Microcontroller.(April 2010, May 2008, Nov 2014) (Or)

   Examine the ADC804 connection to the 8051 in Figure. Write a program to monitor the INTR pin and bring an analog input into register A. Then call a hex-to ACSII conversion and data display subroutines. Do this continuously. (NOV 2007)

7. Explain the DAC interface with 8051. (May 2008,2018,2019) (Or)

Develop 8051 based system having 8Kbyte RAM to generate the triangular wave using DAC. (April 2017,2018)

8. Explain the interfacing of temperature sensor with 8051. **(May 2019)**

9. Describe the external memory and its interfacing with 8051. (NOV 2009, May 2008) (Or)
   Write short notes on memory addressing. (Nov /Dec 2007) (Or)
   How a program memory and a data memory are interfaced with 8051. (NOV 2007) (May 2019**)** (Or)
   Write a brief note on external data move operations in 8051. (May 2016)
10. Demonstrate the interfacing of the stepper motor with 8051 and explain its interfacing diagram and develop to rotate the motor in clock wise direction (April 2017, NOV 2016, May 2016, May 2010, May 2009, May 2008, May 2007, Nov 2017,2015, 2014, 2013, 2011, 2010 & May 2013) (Or)
    Describe in detail the microcontroller based system design with an example. (NOV 2102)
11. Write short notes on PIC microcontrollers.
12. Brief the ARM processor architecture.